REMARKS

Claims 36 and 37 are amended herein to correct typographical errors and antecedent basis. Applicant contends the typographical errors are apparent from the context of the claims and are therefore suitable for correction under 37 C.F.R. §1.312. In claim 36, the third line has been amended to state "forming a lock bit erase enable circuit coupled to the floating gate erase circuit, wherein the ~~erase block~~ lock bit erase enable circuit is operable only when an integrated circuit containing the protection register is in wafer form." In claim 37, the preamble has been amended to state "The method of claim 36, wherein forming the ~~erase block~~ lock bit erase enable circuit further comprises," and the third line amended to state "forming an input buffer, wherein an input of the input buffer is coupled to the bond pad and where an output of the input buffer is coupled to ~~a~~ the floating gate erase circuit." As such, Applicant contends that the amendment raises no new material issues and that no new matter has been added by these corrections.

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2207.

Respectfully submitted,

Date: 6/30/05

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